REMARKS/ARGUMENTS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendments and the following remarks. The Applicants originally submitted Claims 1-20 in the application. In this response, the Applicants have resubmitted Claims 1-20 without amendment. Accordingly, Claims 1-20 are currently pending in the application.

I. Formal Matters and Objections

The Examiner objects to Claims 4, 11 and 18 for failing to provide proper antecedent basis for the claimed subject matter. The Applicants respectfully direct the Examiner to ¶ 50 of the specification, which contains the subject matter of these claims.

The Examiner has objected to the form of the first sentence of the Abstract pursuant to MPEP ¶ 608.01(b), and requires amendment of the sentence. The Examiner has also objected to the use of bold face type in the section headings of the application pursuant to MPEP ¶ 608.01(a) and requests amendment. In addition, the Applicants have identified a typographical error in Table 2 of the Application. In order to clearly communicate these amendments, the Applicants have provided a clean copy of the application, with all amendments, and also a marked up version of the application, and appreciate the Examiner's diligence in bringing these matters to their attention.

The Examiner objects to Claims 1, 8 and 15 for being indefinite with respect to the term "younger instructions," but appears to withdraw the objection in paragraph 13 of the communication. The Applicants interpret paragraph 13 to mean that the objection is withdrawn, and that no action on the part of the Applicants is required regarding this objection.

II. Required Drawing Amendments

The Examiner has objected to the drawings on various grounds as follows:

1) Figure 1: should be designated as prior art. The Figure has been amended as requested.

2) Figure 2: DEU/ETM shown in the drawing is not mentioned in the description of the drawing. This feature is not relevant to the claimed invention, and has been deleted from Fig. 2.

3) Not every feature of Claims 6, 12, 13, 19 and 20 is shown in the drawings: The features claimed in these Claims are all embodied in Fig. 6. Regarding Claim 6, "wherein grouping logic within said processor groups said multiply-accumulate instructions based on said mechanism" is embodied in block 620 of the flowchart shown in Fig. 6. Grouping logic is also pictured generally in Fig. 1, element 263. These figure elements similarly support Claims 13 and 20, which use variations of this claim language to claim the same element of the invention. Regarding Claim 5, 12 and 19, "interim results are unavailable to an external program executing in said DPS" is inherent in the functioning of block 640 of Fig. 6, inasmuch as writeback of the interim results to one or more registers in the ORF does not make the interim results available to an external program executing in the DSP. This feature is addressed in detail in ¶ 50 of the detailed description.

4) The word "FIGURE" should be replaced in all drawings with "FIG." The figures have been amended as requested.

5) Requirement to replace handwritten notation in Figs. 1-6 with its typed equivalent: 37 CFR § 1.84(l) does not require typewritten notation. The rule requires "All drawings must be made by a process which will give them satisfactory reproduction characteristics." The drawings submitted by the Applicants meet the requirements of this rule. However, the Applicants have submitted a new sheet containing Figs. 3 and 6 to partially address the Examiner's concerns in this

matter. Figs. 3 and 6 are merely reproduced in typewritten form, and are not amended, other than to replace "FIGURE" with "FIG."

6) The Examiner requests that DSP 100 in Fig.1 be explicitly labeled "DSP 100." The figure has been amended as requested.

Corrected drawing sheets for Figs. 1-6 are provided herewith to meet the Examiner's requirement for such. Notwithstanding the Examiner's statement that the objection to the drawings will not be held in abeyance, the Applicants request that the Examiner do so for any remaining objections until such time as allowable subject matter is identified by the Examiner.

III. Rejection of Claims 1-20 Under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 1-20 under 35 U.S.C. § 103(a) as being unpatentable over Motorola, Inc. (MPC7410 RISC Microprocessor Technical Summary), in view of Morris (Computer Architecture: The Anatomy of Modern Processors). Specifically, the Examiner asserts that each element of independent Claims 1, 8 and 15 read on the combination of Motorola and Morris, and further, that one of ordinary skill in the art would be motivated to combine Motorola and Morris. More specifically, the Examiner admits that Motorola is silent regarding out-of-order completion logic, but looks to Morris to provide the general background of processor architecture to show that the MPC7410 processor uses pipeline registers. The Examiner continues, referring to the MPC7410 processor in paragraph 22 of the response, "The pipeline registers of the floating-point unit are part of the out-of-order completion logic, associated with said MAC." This assertion is clearly erroneous for the reasons set forth below.

The pipeline registers of the MPC7410 processor cannot be properly construed as out-of-order completion logic, as recited in independent Claims 1, 8, and 15. The present invention

introduces the broad concept of pipelining a MAC and employing logic to support out-of-order completion to allow the MAC to operate at a higher throughput than was previously possible. As illustrated in one embodiment of the invention, the out-of-order completion is supported by out-of-order completion logic that is physically divided between the instruction issue (ISU) block and the write-back (WB) stage of the pipeline. Specification, ¶ 47. Further, the portion of the out-of-order completion logic located in the ISU may be used to group MAC instructions appropriately. Id., ¶ 48. The grouping rules applied by the ISU are shown in Table 2. These rules are a sophisticated logical algorithm designed to efficiently group processor instructions so as to maximize processing speed by maximizing utilization of resources. The grouping algorithm allows instructions to be reordered to achieve the desired resource utilization. Pipeline registers, in contrast, simply store the state of a particular stage in a pipeline for the duration of a single clock period while latencies in the processor settle. Pipeline registers have no ability, inherent or otherwise, to modify the order of operand processing in the processor. Simply put, pipeline registers are not out-of-order completion logic.

As the Examiner has admitted, Motorola is silent regarding out-of-order completion logic. Examiner's Response, ¶ 18-19. Morris is also silent in this regard. Therefore, there is no teaching or suggestion in Motorola or Morris, separately or in combination, of out-of-order completion logic. The combination of these references is therefore improper and fails to sustain a *prima facie* case of obviousness in Claims1, 8, and 15, and these claims are allowable. The remaining claims depend from Claims 1, 8 or 15, and are thus also allowable.

IV. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-20.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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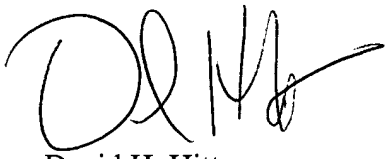

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